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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,862	04/15/2004	Husam N. Alshareef	TI 36557	7108

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EXAMINER	
LEE, CHEUNG	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/824,862	ALSHAREEF ET AL.	
	Examiner	Art Unit	
	Cheung Lee	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) ~~12~~ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1a. Applicant's election without traverse of claims 1-16 in the reply filed on June 23, 2005 is acknowledged.

Claim Objections

1b. Claim 12 is objected to because of the following informalities: the high pressure range is to about 1100 mT, not 11000 mT, according to the specification (page 11, paragraph 24). Appropriate correction is required.

Claim Rejections - 35 USC § 103

1c. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugawara et al. (U.S. Publication 2004/0142577; hereinafter "Sugawara").

3. With respect to claim 1, Sugawara discloses a method for controlling the amount of gate leakage in a semiconductor device, comprising: placing a semiconductor substrate in a plasma chamber (fig. 3, item 32); and subjecting a gate dielectric layer located over said semiconductor substrate (page 3, paragraphs 51-52) to a gas mixture including argon and nitrogen under plasma conditions (page 3, paragraphs 52 and 54),

but Sugawara does not disclose expressly wherein a flow rate of said argon ranges from about 1700 sccm to about 2200 sccm and a flow rate of said nitrogen ranges from about 40 sccm to about 200 sccm. However, Sugawara discloses the preferable nitrogen flow rate from 4 sccm to 200 sccm (page 3, paragraph 57), and the preferable argon flow rate from 1000 sccm to 2000 sccm (page 3, paragraph 58). In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F. 2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F. 2d 1575, 16 USPQ 2d 1934 (Fed. Cir. 1990).

4. With respect to claim 11, Sugawara discloses a method of forming a gate dielectric in a plasma chamber, comprising: placing a semiconductor substrate (page 2, paragraph 36) in a plasma chamber (page 6, paragraphs 132 and 133); forming a gate dielectric layer over said semiconductor substrate (page 2, paragraphs 35-38); subjecting said gate dielectric within said plasma chamber to a gas mixture including argon and nitrogen under plasma conditions (page 3, paragraphs 51-54) and under high pressure (page 3, paragraph 61), but Sugawara does not disclose expressly wherein a flow rate of said argon ranges from about 1700 sccm to about 2200 sccm and a flow rate of said nitrogen ranges from about 40 sccm to about 200 sccm. Sugawara discloses argon flow rate ranges from 200 sccm to 2000 sccm (page 3, paragraph 58), and nitrogen flow rate ranges from 2 sccm to 500 sccm (page 3, paragraph 57). The arguments concerning overlapping range stated in claim 1 also apply.

5. With respect to claim 2, Sugawara discloses a method for controlling the amount of gate leakage in a semiconductor device as set forth in claim 1, but Sugawara does

not disclose expressly wherein said subjecting is conducted at a pressure ranging from about 700 mT to about 1100 mT. Sugawara discloses a nitridation pressure range from 10 mT to 3000 mT (page 3, paragraph 61). The arguments concerning overlapping range stated in claim 1 also apply.

6. With respect to claim 12, Sugawara discloses a method of forming a gate dielectric as set forth in claim 11, but Sugawara does not disclose expressly wherein said high pressure ranges from about 700 mT to about 11000 mT. Sugawara discloses nitridation pressure range from 10 mT to 3000 mT (page 3, paragraph 61). The arguments concerning overlapping range stated in claim 1 also apply.

7. With respect to claim 3, Sugawara discloses a method for controlling the amount of gate leakage in a semiconductor device as set forth in claim 2, further including adjusting a flow rate of said argon and said nitrogen and a pressure of said plasma conditions to provide a desired gate leakage of said semiconductor device (page 3, paragraphs 63-67). Sugawara discloses an example parameters for the preferred condition to process nitridation (page 3, paragraphs 63-67). According to the examples of preferred conditions, it is obvious that Sugawara adjusts parameters to provide a desired gate leakage under preferred plasma condition.

8. With respect to claim 4, Sugawara discloses a method for controlling the amount of gate leakage in a semiconductor device as set forth in claim 3, wherein said desired gate leakage is achieved while maintaining a targeted equivalent oxide thickness (fig 9, graph 2; page 9, paragraphs 190-195). As shown by graph 2 in figure 9, the gate leakage is very low within low equivalent film thicknesses, and these results provide a

high-performance semiconductor structure having a good electric characteristic sufficient to apply to an industrial use (page 9, paragraphs 191-195).

9. With respect to claims 5 and 14, Sugawara discloses a method for controlling the amount of gate leakage in a semiconductor device as set forth in claim 1 and a method of forming a gate dielectric as set forth in claim 11, but Sugawara does not disclose expressly wherein a power of said plasma ranges from about 800 watts to about 1000 watts (to about 1400 watts, pertaining to claim 14) and a temperature of said semiconductor substrate ranges from about 300°C to about 500°C. Sugawara discloses a preferable temperature ranges from 200°C to 500°C (page 3, paragraph 60). The arguments concerning overlapping range stated in claim 1 also apply. Also, Sugawara discloses a microwave power from 0.5 W/cm^2 to 4 W/cm^2 (page 3, paragraph 62). The examiner takes the position that it is obvious that Sugawara's power range is within the claimed limitation since other Sugawara's plasma condition parameters are within the claimed parameters.

10. With respect to claim 6, Sugawara discloses a method for controlling the amount of gate leakage in a semiconductor device as set forth in claim 1, wherein subjecting is conducted in a microwave chamber (page 6, paragraphs 132 and 133), but Sugawara does not disclose expressly wherein subjecting conducted in a presence of oxygen. However, Sugawara performs an oxidation treatment using oxygen to form an oxide film (page 2, paragraphs 35-44), and Sugawara does not disclose that the plasma chamber has 100% vacuum condition during the nitridation. So, the examiner takes the position

that it is inherent that the nitridation is conducted in a presence of oxygen due to the presence of residual oxygen in the chamber.

11. With respect to claims 7, 8, and 15, Sugawara discloses a method for controlling the amount of gate leakage in a semiconductor device as set forth in claim 1 and a method of forming a gate dielectric as set forth in claim 11, but Sugawara does not disclose expressly wherein a flow of said argon is about 1950 sccm and a flow of said nitrogen is about 100 sccm. However, Sugawara discloses a range of argon flow from 200 sccm to 2000 sccm (page 3, paragraph 58) and a range of nitrogen flow from 2 sccm to 500 sccm (page 3, paragraph 57). The arguments concerning overlapping range stated in claim 1 also apply.

12. With respect to claims 9 and 10, Sugawara discloses a method for controlling the amount of gate leakage in a semiconductor device as set forth in claim 1, but Sugawara does not disclose expressly wherein said subjecting results in a semiconductor device wherein a concentration of nitrogen within said gate dielectric layer ranges from about 5% to about 15% and an equivalent oxide thickness of said gate dielectric layer is about 1.25 nm and a gate leakage of said gate dielectric layer ranges from about 30 A/cm^2 to about 80 A/cm^2 (pertaining to claim 9), and said concentration of said nitrogen 11% (pertaining to claim 10). Sugawara shows nitrogen concentration after nitridation was conducted ranging from about 2.5% to about 18%, at most 20% as shown in figure 10 (fig. 10; page 5, paragraphs 105 and 106). The electric film thickness (equivalent oxide film thickness) ranges from 1.0 nm to 2.5nm (page 5, paragraph 110). And as shown in figure 9, the leakage of the gate dielectric layer increases by increasing nitridation

period, so with enough nitridation time, the gate leakage will range within the claimed leakage range. The arguments concerning overlapping range stated in claim 1 also apply.

13. With respect to claim 13, Sugawara discloses a method of forming a gate dielectric as set forth in claim 11, further including adjusting a flow rate of said argon and said nitrogen and a pressure of said plasma conditions to provide a desired gate leakage of said semiconductor device (page 3, paragraphs 63-67), wherein said desired gate leakage is achieved within a targeted equivalent oxide thickness (fig 9, graph 2; page 9, paragraphs 190-195), but Sugawara does not disclose expressly wherein desired gate leakage is achieved in a presence of oxygen. Sugawara discloses an example parameters for the preferred condition to process nitridation (page 3, paragraphs 63-67). Also, as shown by graph 2 in figure 9, the gate leakage is very low within low equivalent film thicknesses, and these results provide a high-performance semiconductor structure having a good electric characteristic sufficient to apply to an industrial use (page 9, paragraphs 191-195). According to the examples of preferred conditions, it is obvious that Sugawara adjusts parameters to provide a desired gate leakage within a targeted equivalent oxide thickness under preferred plasma condition. Sugawara performs an oxidation treatment using oxygen to form an oxide film (page 2, paragraphs 35-44), and Sugawara does not disclose that the plasma chamber has 100% vacuum condition during the nitridation. So, the examiner takes the position that it is inherent that a desired gate leakage is achieved in a presence of oxygen due to the presence of residual oxygen in the chamber.

14. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sugawara, as applied to claim 11 above, in view of second Sugawara et al. (U.S. Publication 2005/0161434; hereinafter "Sugawara2").

With respect to claim 16, Sugawara discloses a method of forming a gate dielectric as set forth in claim 11, further including: forming a gate layer over gate dielectric layer (page 3, paragraph 70; page 9, paragraph 193; page 10, paragraph 198), but Sugawara does not disclose expressly patterning said gate layer and said gate dielectric layer into a plurality of transistor gates; forming source/drains in well regions associated with each of said plurality of said transistor gates, said well region being located in said semiconductor substrate and between isolations regions located between said transistor gates; forming dielectric layers over said transistor gates; and forming interconnects in and between said dielectric layers to interconnect said transistor gates to form an operative integrated circuit.

Sugawara2 discloses a similar method of forming a gate dielectric as set forth in claim 11, wherein forming a film of polysilicon as a gate electrode (fig. 13, page 9, paragraph 159) then patterning of the gate and selective etching to form a transistor gate (fig. 14; page 9, paragraph 160); forming a source/drain in well region associated with a transistor gate, said well region being located in said semiconductor substrate and between isolation regions (fig. 15; page 9, paragraph 160); forming dielectric layers over said transistor gate (page 9, paragraph 160); and forming interconnects in and between said dielectric layers to interconnect said transistor gate to form an operative

integrated circuit (figures 15-16; page 9, paragraph 160). Sugawara only discloses the forming of one transistor gate, but it would have been obvious to simultaneously form a plurality of transistor gates on a semiconductor substrate to reduce fabrication cost and time.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine Sugawara2 with Sugawara to form interconnected devices forming a complete operative integrated circuit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cheung Lee whose telephone number is 571-272-5977. The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cheung Lee

August 15, 2005

HA NGUYEN
PRIMARY EXAMINER